REMARKS

The present invention is directed to a highly competitive area in the manufacture of semi-conductor elements where high speed and cost are part of the basic design requirements. The present invention is addressing the requirement to provide high frequency components in, for example, a portable terminal such as a monolithic microwave IC (MMIC). In such an environment, both active and passive elements form circuits that are required to be grounded.

The Office Action cited Figs. 8C and 8D of our application in combination with the *Yeh et al.* (U.S. Patent No. 6,294,834) to contend that each of the outstanding claims 10, 11, and 27-30 would be obvious under 35 U.S.C. §103. Figures 8C and 8D disclose basically conventional RF circuits equipped with via-holes. Specifically, Figure 8C discloses a pattern diagram of an RF passive circuit with a via-hole 821. A spiral electrode pattern is formed on a GaAs substrate and connected by virtue of a contact hole 833 with a wiring metal layer 831. As can be appreciated, the conventional form of RF amplifiers and RF passive circuits are limited in the reduction size due to the two-dimensional positioning of the elements of a drain voltage feeding circuit 807 as shown in Figure 8A.

The present invention utilizes a three-dimensional location of a spiral inductor, a capacitor and a via-hole, thereby enabling a smaller passive RF circuit and RF amplifier wherein the RF amplifier can include an RF choke that is used in at least one of a matching circuit and a bias feeding circuit.

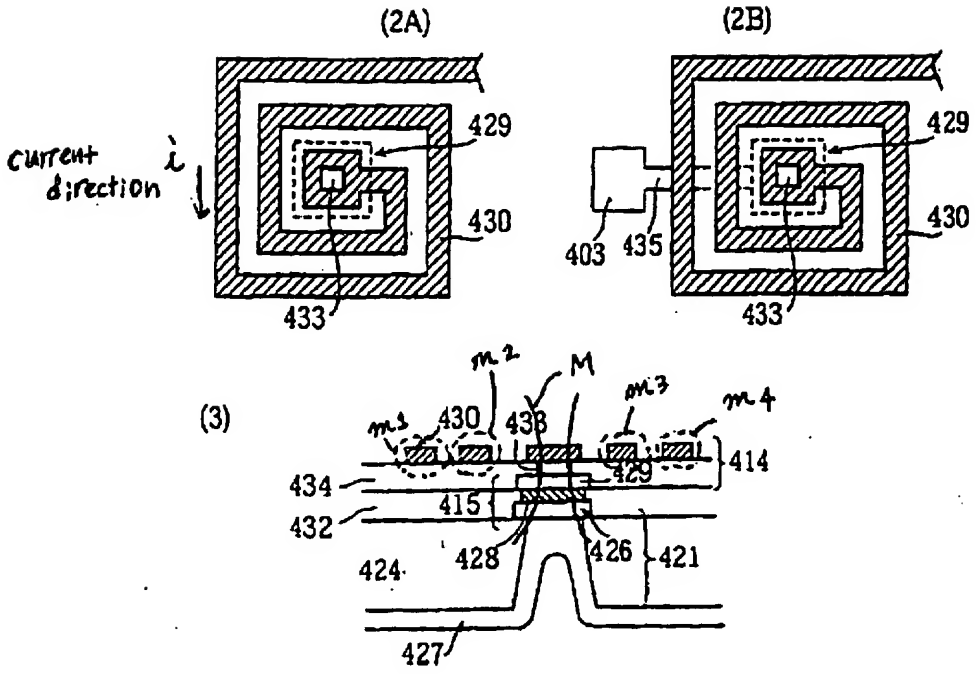
As shown in our selected embodiment of Figures 4A-D, an input matching circuit via-hole is placed underneath the center of a spiral pattern of an input matching parallel inductor. Additionally an MIM capacitor is formed in alignment with both a contact hole connecting to the inductor, and also in direct alignment with the via-hole formed from the back side of the

substrate. One end of the capacitor can be grounded while connecting the other end to the inductor which forms the equivalent input matching circuit portion 425 in Figure 4A. These features are set forth in the amended claims 10 and 11.

An advantageous feature of our present invention is the placement of the via-hole beneath and aligned with the center of our spiral formed metal layer. The metal layer or wiring pattern forms an inductance component in a spiral configuration. A MIM capacitor is also provided to be aligned with the center of the spirally-formed metal layer.

If a via-hole is formed as shown in the prior art Figures 8A-8D cited in the Office Action rejection, the wiring from the spiral inductor to the via-hole would be unnecessarily long and can cause an unnecessary inductance component which may lead to an impedance mismatch. The present invention can prevent such a phenomena since the wiring from the center of the spiral inductor to the via-hole is now minimized.

In addition, any field distribution for a spiral inductor under a high frequency operation has a vertical-direction component in the horizontal plane of the spiral inductor and is strong in the center-vicinity of the spiral inductor when the current i runs in the direction (see arrow Figure 2A below) and the field distribution can be represented by m1, m2, m3, m4 and M (see Figure 3). Broken lines are utilized to indicate the field distribution m1, m2, m3 and m4 for each line constituting the spiral inductor while the solid line, M, provides the compound field distribution in the center-vicinity in which the field distributions from all the lines are incorporated.

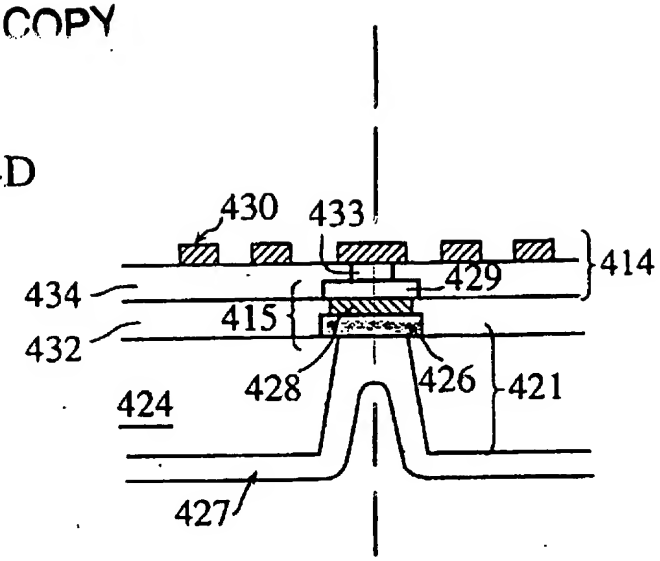


Thus, as can be seen above, if the via-hole is provided in a position apart from the center of the spiral inductor, there is a chance of disturbing the field distribution to inhibit a desirable inductance component. Additionally, the objectives of a compact and economically three dimensional configuration is provided while addressing the grounding issue in our invention.

The *Yeh et al.* reference sought to provide technology that would be compatible with conventional VLSI technology while incorporating a combination of a dual damascene formation of grooves and SOI technology to reduce parasitic capacitance.

As shown in Figure 1, a via opening 44 enables a connection with one side of an inductor 11 to an offset capacitor 32. Resistive material 20 and 22 connect the other side of the capacitor 32 to the node point 1 at the top of the via-hole 42. A pair of via-holes 46 and 48, shown in Figure 1, connects the capacitor's lower electrode to a transistor 24. This arrangement is not equivalent to the structure of our Figure 4D as follows.

Fig.4D



As can be determined, a central alignment of the via-hole, capacitor and the center of the spiral inductor provides a more compact structure while addressing the problem of any unnecessary inductance component from the wiring connections.

The *Yeh et al.* reference produces a inductance component by means of a wiring metal layer in a linear form and it further does not teach nor disclose that its via-hole is positioned in the center of a spiral inductor. There certainly is no teaching in our present description of relevant art Figure 8 cited in the Office Action that would suggest that a via-hole be provided in the center vicinity of the spiral inductor. The *Yeh et al.* reference Figure 1 also discloses that this issue is neither addressed nor taught in this reference.

Even if a person of ordinary skill in the field had both of these references before him/her, the person would not be informed of the desirability of the circuit structure as now set forth in our amended claims 10 and 11 and new claim 31.

It should be noted that the burden of establishing a *prima facie* case of obviousness lies with the Patent Office. *In 're Fine*, 5 USPQ2d (Fed. Cir. 1988) (stating: "The PTO has the burden under section 103 to establish a *prima facie* case of obviousness"). To establish a *prima facie* case of obviousness, (1) there must be some suggestion or motivation (either in the references themselves or in the knowledge generally available to one of ordinary skill in the art)

to combine the reference teachings; (2) there must be a reasonable expectation of success; and (3) the prior art reference must teach or suggest all the claim limitations. See *MPEP §§* 2142-43.

In view of the above amendments and the submission of new Claim 31, it is believed the case is in condition for allowance. Even if a person of ordinary skill had both of the cited prior art disclosures before them, these references certainly would not teach the advantageous position of aligning a via-hole concentric with the center of the spirally-formed metal layer of the inductor nor would they teach an MIM capacitor forming an input matching capacitor aligned with and between the inductor and the via-hole as disclosed and described in the new Claims 31 and 32.

It is believed that the case in now in condition for allowance and an early notification of the same is requested.

If there are any questions with regard to the prosecution of this matter, the undersigned attorney can be contacted at the listed telephone number.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on June 22, 2005.

By: Sharon Farnus

Signature

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Very truly yours,

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